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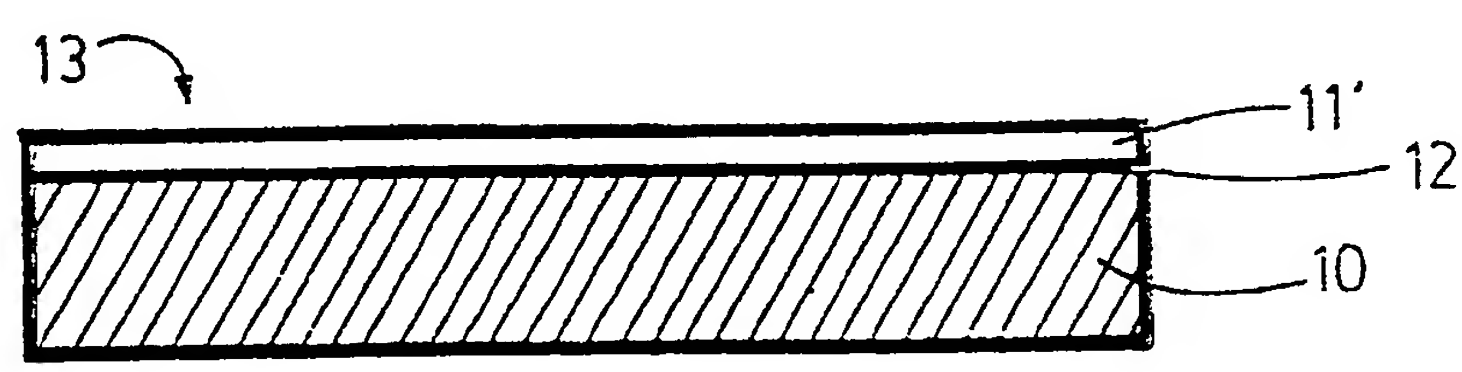
(54) Title: FABRICATION OF ULTRA-LOW EXPANSION SILICON MASK BLANKS



(57) Abstract: A method for fabricating masks for extreme ultraviolet lithography (EUVL) using Ultra-Low Expansion (ULE) substrates and crystalline silicon. ULE substrates are required for the necessary thermal management in EUVL mask blanks, and defect detection and classification have been obtained using crystalline silicon substrate materials. Thus, this method provides the advantages for both the ULE substrate and the crystalline silicon in an Extreme Ultra-Violet (EUV) mask blank. The method is carried out by bonding a crystalline silicon wafer or member to a ULE wafer or substrate and thinning the silicon to produce a 5-10 µm thick crystalline silicon layer on the surface of the ULE substrate. The thinning of the crystalline silicon may be carried out, for example, by chemical mechanical polishing and if necessary or desired, oxidizing the silicon followed by etching to the desired thickness of the silicon.

WO 01/75522 A1

FABRICATION OF ULTRA-LOW EXPANSION SILICON MASK BLANKS

BACKGROUND OF THE INVENTION

The present invention is related to the fabrication of mask blanks for lithographic applications, particularly to fabricating mask blanks for Extreme Ultra-Violet Lithography (EUVL) and more particularly to a method for fabricating EUVL mask blanks composed of an Ultra-Low Expansion (ULE) substrate with a crystalline silicon surface.

EUVL is a leading candidate for the next generation of lithographic systems for fabrication of semiconductor microelectronics. EUVL technology development is progressing toward insertion into the production of integrated circuits with critical dimensions of 70 nm. The key difference between EUVL and conventional lithography is that the EUVL employs 13.4 nm light and therefore requires reflective optics that are coated with multilayers, typically alternating layers of molybdenum and silicon (Mo/Si). Deposition of low defect, uniform multilayer coatings on mask blanks is an area of intense development. Also, development of mask blanks or substrates that enable inspection for defects is another area of current development.

Thermal management of EUVL masks or substrates has become an important field in view of the current development efforts relating to EUVL systems. ULE materials, such as glass substrates, which have thermal coefficient advantages compared to silicon substrates, are being considered for the thermal management in EUVL mask blanks. Also, the vast experience with fabrication and processing, including the defect detection and classification results that have been obtained using crystalline silicon substrate materials, render crystalline silicon a desirable material for EUVL masks. Since mask blank defect inspection is one of the most important factors in determining mask blank yield and, as a consequence cost, the use of ULE mask blanks with a crystalline silicon surface is of great value to the EUVL program.

Various techniques for bonding silicon wafers to silicon or other materials

are known in the art and include thermal-compression, anodic, etc. The bonding of silicon to a substrate can also be carried out at various temperatures including room temperature bonding. See S. N. Farren's et al., Chemical Free Room Temperature Wafer to Wafer Direct Bonding, J. Electrochem. Soc. Vol. 142, No. 1, November 1995, 3949 – 3955.

The present invention provides a method that produces a mask blank which incorporates the thermal coefficient advantages of ULE substrates and the defect detection and classification advantages of crystalline silicon. The mask blanks composed of a ULE substrate with a crystalline silicon surface produced by the fabrication method of the present invention are applicable for EUVL systems now under development. Basically the fabrication method involves bonding a crystalline silicon wafer to a ULE wafer and thinning the crystalline silicon to a thickness of about 5-10 μm.

Summary of the Invention

It is an object of the present invention to provide an Extreme Ultra-Violet Lithography (EUVL) mask blanks using Ultra-Low Expansion (ULE) mask substrates.

A further object of the invention is to provide an EUVL mask blank wherein defect detection can be effectively carried out.

Another object of the invention is to provide ULE/silicon (ULE/Si) Extreme Ultra-Violet (EUV) mask blanks.

Another object of the invention is to provide a method for fabricating mask blanks composed of an ULE substrate with a crystalline silicon surface.

Another object of the invention is to provide a mask blank which combines the advantages of ultra-low thermal expansion of selected materials such as glass, plastics, and ceramics with the defect inspection advantages of crystalline silicon.

Another object of the invention is to provide a method for fabricating EUVL mask blanks by bonding a crystalline silicon wafer to an ULE wafer and thinning the

silicon wafer to a thickness of about 5-10 μm crystalline silicon film.

Other objects and advantages of the present invention will become apparent from the following description and accompanying drawings. The invention involves a method for the fabrication of ultra-low expansion/silicon extreme ultraviolet mask blanks. The ULE substrate enables the necessary thermal management in EUVL mask blanks while the silicon surface film on the substrate enables defect inspection, which is one of the most important factors in determining mask blank yield and as a consequence, cost, of the mask blank. By combining ULE/Si into a mask blank, there is produced an effective EUV mask blank on which reflective multilayers may be deposited for EUVL applications. Basically the method involves bonding a crystalline silicon wafer to an ultra-low expansion wafer such as selected glass, plastic or ceramic and then thinning the silicon to a desired thickness (e.g., 5-10 μm). The silicon can be thinned and polished by chemical and mechanical polishing and thermal oxidation followed by etching, where needed, to produce a crystalline silicon surface on the ULE substrate.

Brief Description of the Drawings

The accompanying drawings, which are incorporated into and form a part of the disclosure, illustrate embodiments of the invention and together with the description, serve to explain the principles of the invention.

Figures 1A, 1B and 1C illustrate the method of the invention utilizing chemical mechanical polishing to thin a silicon wafer bonded to an ultra-low expansion wafer to produce the mask blank of Figure 1C.

Figures 1D and 1E illustrate the oxidation and etching operations on a polished silicon wafer, such as in Figure 1C, for thinning the silicon to produce the ULE/Si mask blank of Figure 1E.

Detailed Description of the Invention

The present invention is directed to a method for fabricating masks for

Extreme Ultra-Violet Lithography (EUVL). The invention is based on two factors: first Ultra-Low Expansion (ULE) substrates are required for the necessary thermal management in EUVL mask blanks; and second the vast experience with fabrication and processing including defect detection and classification results that have been obtained using crystalline silicon substrate materials. Since Extreme Ultra-Violet (EUV) mask blank defect inspection is one of the most important factors in determining mask blank yield and as a consequence, cost, the use of EUV mask blanks with a crystalline silicon surface is of great value to the EUV systems. By combining the advantages of ULE substrates and crystalline silicon surfaces, thermal management and defect inspection problems for EUVL mask blanks can be resolved or greatly reduced. ULE material is defined as a material with a coefficient of thermal expansion <100 ppk/°K, and may be composed of selected glass, plastic or ceramic.

The method of the present invention is herein after described with reference to Figures 1A through 1E. In this described, and illustrated example of the method, a ULE wafer 10 and a crystalline silicon wafer 11 of the same diameter are provided, as shown in Figure 1A, which may be for example about 8 inches (20.3 cm) in diameter. The ULE wafer may have, for example, a thickness of about 0.25 inches (0.64 cm) and the silicon wafer a thickness of about 0.025 inches (650 μm), although the thickness of the ULE wafer may vary from about 0.2 inches (0.5 cm) to about 0.5 inches (1.3 cm) and the thickness of the silicon wafer from about 600 μm to about 800 μm. Next, the silicon wafer 11 is bonded to ULE wafer 10 as indicated at 12, as shown in Figure 1B, by conventional bonding techniques such as anodic, thermal compression, room temperature, etc., each of which is commonly known in integrated circuit fabrication. The silicon wafer 11 is then ground and polished using for example, chemical and mechanical polishing to a thickness of about 5 μm to about 10 μm for example as shown in Figure 1C, whereby a mask blank composite at 13, composed of a ULE substrate with a crystalline silicon surface having a 5-10 μm thickness is produced.

Additional silicon wafer thinning, if necessary, is achieved by oxidizing the silicon 11 to produce an SiO_2 film 14 on silicon 11 as shown in Figure 1D followed by etching with a buffered hydrofluoric acid etch to produce, for example, a 5 μm silicon thickness, 11' as shown in Figure 1E. In fact, oxidation "thinning" is often used to reduce the number of defects (caused by polishing) in silicon wafers used in high volume integrated circuit manufacturing. Note that the final silicon surface, 11 and 11' of Figures 1C and 1E are crystalline.

As set forth above, the primary advantage of crystalline silicon as the top surface is the knowledge base of defect detection and defect mitigation that has been performed on bare crystalline silicon to date. If, on the other hand, silicon is deposited on to the ULE substrate using one of many typical vapor deposition techniques (e.g., sputtering, evaporation, CVD, etc.) then the deposited silicon will likely have an amorphous structure, i. e., amorphous silicon (a-Si) which is undesirable.

One concern associated with the mask blanks produced by the method of this invention is the thermal stress that develops during a thermally activated wafer bonding process. Typically, a thermal compression wafer bonding process operates at around 400°C. Thermal stresses result from cooling two materials with different coefficients of linear thermal expansion (α_L). In addition, the α_L of silicon and ULE materials vary with temperature. However, ULE material can be fabricated to have a desired α_L at a specific temperature by varying to amount of material components. Since the ULE material may, for example, be a ceramic alloy consisting primarily of fused quartz and TiO_2 and the α_L at a given temperature is a strong function of $\%TiO_2$, the α_L can be tailored to match silicon within a specific temperature range. By way of example, TiO_2 might be present in a percentage of between about 0.1% to about 10%. Also, since silicon wafers can be bonded at room temperature, as set forth in the above referenced article by S. N. Farrens, et. al.,

the thermal stress concerns may be reduced dramatically. It is also possible to reduce interface stresses by thermally growing an oxide on the silicon surface which would serve as a "pad" oxide by being more closely matched in α_L to the ULE material, compared to silicon. Thus, after the silicon wafer has been thinned to the desired thickness as shown in Figures 1C and 1E, a film of SiO_2 may be deposited on the silicon 11'.

It has thus been shown that the method of the present invention enables fabrication of ULE/Si EUV mask blanks. By the present method a mask blank is fabricated using a ULE substrate with a crystalline silicon surface which provides the necessary thermal management and defect inspection required by EUVL mask blanks.

While a particular sequence of operations using particular techniques, parameters and materials has been described and illustrated to exemplify and teach the principles of the invention such are not intended to be limiting. Modifications and changes may become apparent to those skilled in the art and it is intended that the invention be limited only by the scope of the appended claims.

CLAIMS

What is claimed is:

1. A method for fabricating mask blanks for use in extreme ultraviolet lithography, comprising;

providing a wafer of an ultra-low expansion material;

providing a wafer of crystalline silicon;

bonding the wafer of crystalline silicon to the wafer of ultra-low expansion material;

reducing the thickness of the wafer of crystalline silicon to a thickness of between about 5 μm and 10 μm; and

polishing the surface of the reduced thickness crystalline silicon thereby forming a mask blank of ultra-low expansion material with a crystalline silicon surface.

2. The method of claim 1 or 2 additionally including forming an oxide film on the crystalline silicon surface for reducing thermal stress.

3. The method of claim 1 or 2 additionally including forming the wafer of ultra-low expansion material from materials selected from the group consisting of glass, plastic and ceramic.

4. The method of claim 1, additionally including forming the wafer of ultra-low expansion material from fused quartz and TiO_2 to form a ceramic wafer.

5. The method of claim 4, additionally including controlling the percentage of TiO_2 to adjust the coefficient of linear thermal expansion of the formed ceramic wafer.

6. The method any of claims 1-3, additionally including controlling the coefficient of expansion of the wafer of ultra-low expansion material by controlling the composition of the material.

7. The method of any preceding claim, wherein the bonding is carried out by a technique selected from the group consisting of anodic bonding, thermal compression bonding, and room temperature bonding.

8. The method of any preceding claim, wherein reducing the thickness of wafer of crystalline silicon and polishing the reduced thickness surface is carried out by chemical and/or mechanical polishing.

9. The method of claim 8, additionally including further thinning of the thickness of the wafer of crystalline silicon to a thickness of about 5 μm by oxidation and etching techniques.

10. The method of claim 9, wherein oxidation of the reduced thickness crystalline silicon is carried out in an oxidation furnace.

11. The method of claim 9, wherein etching of the reduced thick crystalline silicon is carried out with a buffered hydrofluoric acid etch.

12. An ultra-low expansion/crystalline silicon mask blank, particularly applicable for use in extreme ultraviolet lithography systems, comprising:

a substrate of ultra-low expansion material; and

a thin layer of crystalline silicon bonded to a surface of the substrate.

13. The mask blank of claim 12, wherein said substrate of ultra-low expansion material is composed of material selected from the group consisting of glasses, plastics and ceramics.

14. The mask blank of claim 12, wherein said substrate of ultra-low expansion material is a ceramic.

15. The mask blank of claim 14, wherein said ceramic material is composed of fused quartz and TiO_2.

16. The mask blank of claim 15, wherein said ceramic material has a coefficient of linear thermal expansion based on the percentage of TiO_2 therein.

17. The mask blank of claim 16, wherein said percentage of TiO_2 is in the range of between about 0.1% to 10%.

18. The mask of any of claims 12-17, wherein the layer of crystalline silicon has a thickness of 10 microns or less.

19. A method for fabricating EUV mask blanks composed of ULE/Si, comprising:

bonding a wafer of crystalline silicon to a surface of a wafer of ULE material by a technique selected from the group consisting of anodic bonding, thermal compression bonding and room temperature bonding; and

thinning the wafer of crystalline silicon to a thickness of between about 5 μm to about 10 μm.

20. The method of claim 19, wherein the thinning of the wafer of crystalline silicon is carried out by chemical and/or mechanical polishing.

21. The method of claim 19, wherein the thinning of the wafer of crystalline silicon is carried out by chemical and/or mechanical polishing followed by oxidation and etching of the crystalline silicon.

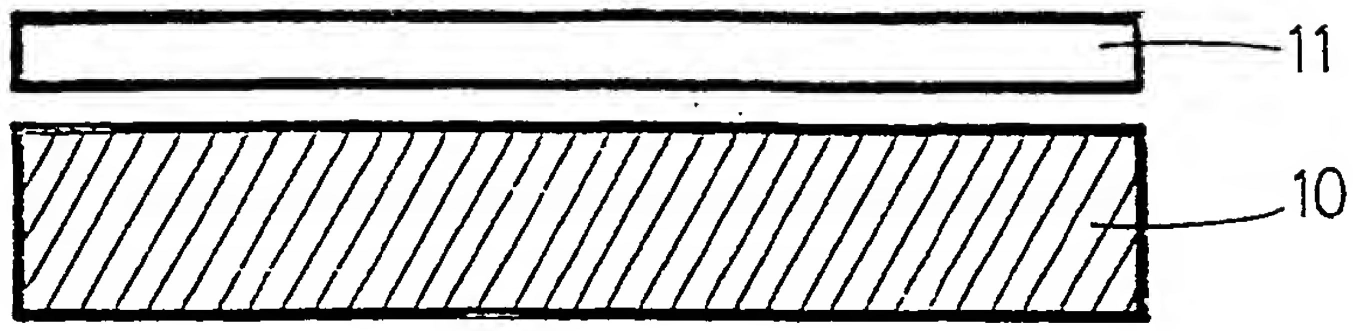


FIG._1A.

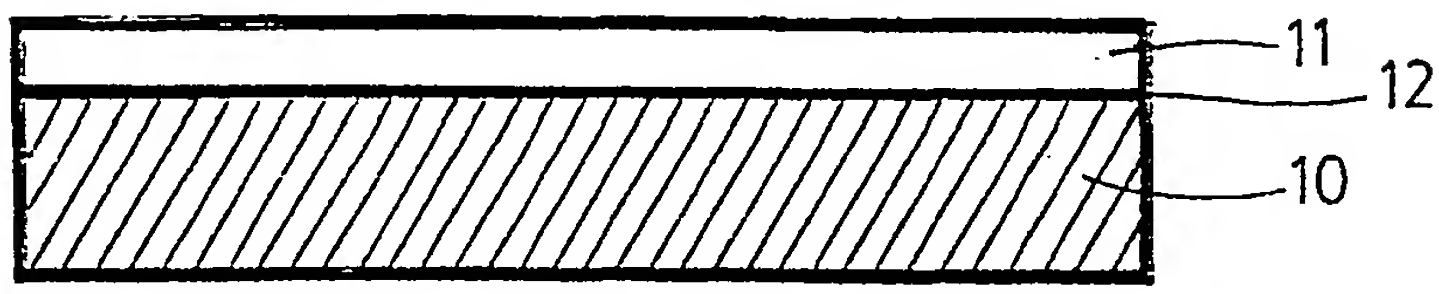


FIG._1B.

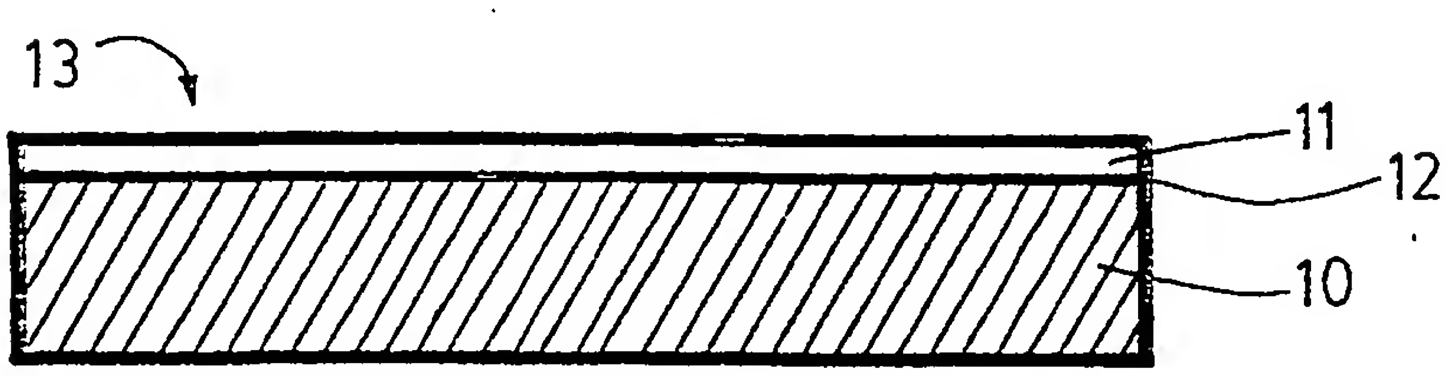


FIG._1C.

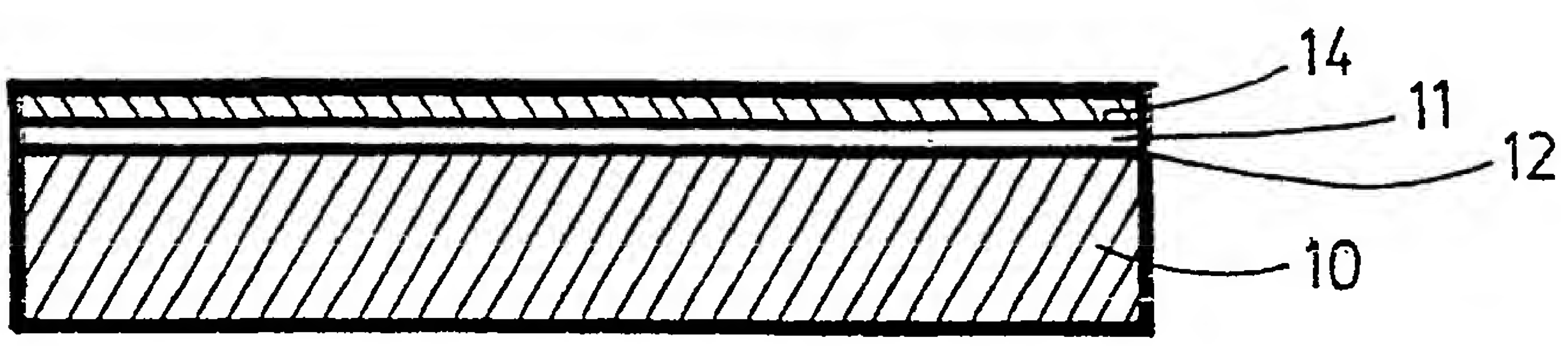


FIG._1D.

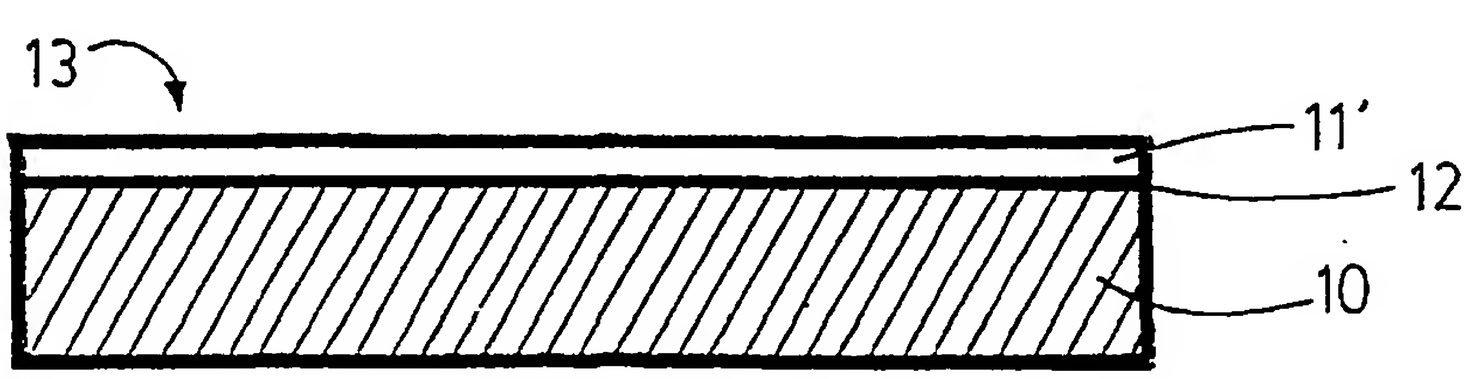


FIG._1E.

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G03F1/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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X	US 4 301 237 A (BURNS JOHN A) 17 November 1981 (1981-11-17) column 4, line 1 - line 4	12

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
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International Application No
PCT/US 01/08426

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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Supp IDS
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Information on patent family members

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